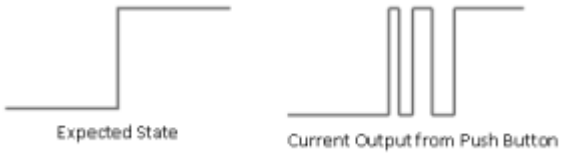
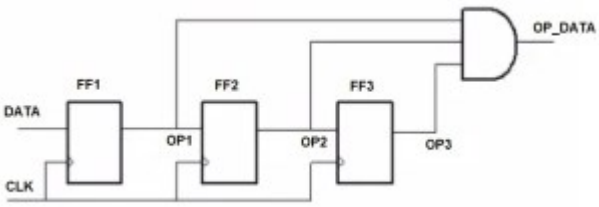
Push Button always got the mechanical property of bouncing state at micro sec.



Debounce output in FPGA

The above figure describes the debouncing output result, when the Push Button is pressed.

When you pull down the push button from high to low state. It bounce back to high and low few times before it settle at proper output. In order to avoid such bouncing state, we need to create debounce logic circuit.



Debounce Logic Circuit

VHDL Code for Debounce Circuit in FPGA

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity VHDL_Code_Debounce is
Port (
DATA: in std_logic;
CLK : in std_logic;
OP_DATA : out std_logic);
end VHDL_Code_Debounce ;

architecture Behavioral of VHDL_Code_Debounce is
```

```
Signal OP1, OP2, OP3: std_logic;

begin

Process(CLK)

begin

If rising_edge(CLK) then

OP1 <= DATA;

OP2 <= OP1;

OP3 <= OP2;

end if;

end process;

OP_DATA <= OP1 and OP2 and OP3;

end Behavioral;
```

Above VHDL Code describes the method to avoid push Button debouncing. Instead of assigning the input data of push button to output, here 3 signals assigned OP1,OP2,OP3 and they all ANDed together and assigned to the output data.