Contents

Clock Divider

Clock Divider is also known as frequency divider, which divides the input clock frequency and produce output clock. In our case let us take input frequency as 50MHz and divide the clock frequency to generate 1KHz output signal.

VHDL code consist of Clock and Reset input, divided clock as output. Count is a signal to generate delay, Tmp signal toggle itself when the count value reaches 25000. Output produce 1KHz clock frequency.

Reference count values to generate various clock frequency output

Count Value	Output Frequency
1	25MHz
25	1MHz
50	500KHz
1000	25KHz
25000000	1Hz

VHDL Code for Clock Divider

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.numeric_std.ALL;

entity Clock_Divider is
port ( clk,reset: in std_logic;
clock_out: out std_logic);
end Clock_Divider;

architecture bhv of Clock_Divider is

signal count: integer:=1;
signal tmp : std_logic := '0';

begin

process(clk,reset)
begin
if(reset='1') then
count<=1;
tmp<='0';
elsif(clk'event and clk='1') then
count <=count+1;
if (count = 25000) then
tmp <= NOT tmp;
count <= 1;
end if;
end if;
clock_out <= tmp;
end process;

end bhv;
```

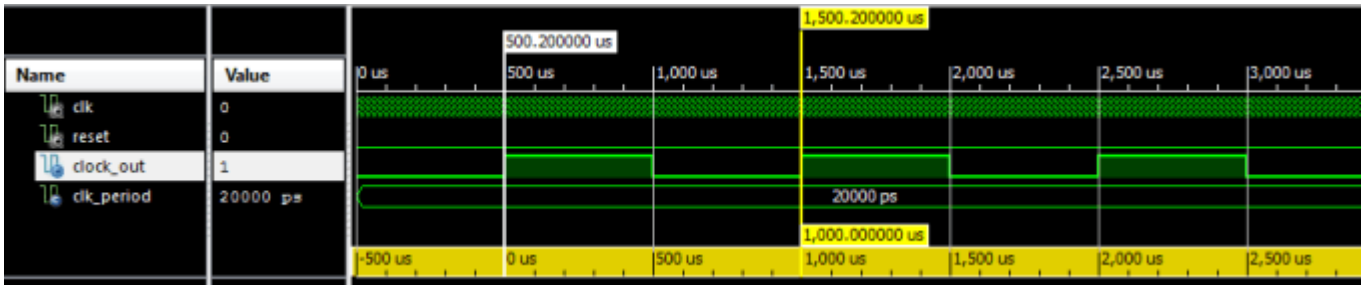
VHDL Testbench code for Clock Divider

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Tb_clock_divider IS
END Tb_clock_divider;

ARCHITECTURE behavior OF Tb_clock_divider IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT Clock_Divider
PORT(
clk : IN std_logic;
reset : IN std_logic;
clock_out : OUT std_logic
);
END COMPONENT;

--Inputs
signal clk : std_logic := '0';
signal reset : std_logic := '0';

--Outputs
signal clock_out : std_logic;

-- Clock period definitions
constant clk_period : time := 20 ns;

BEGIN
```

```
-- Instantiate the Unit Under Test (UUT)
uut: Clock_Divider PORT MAP (
clk => clk,
reset => reset,
clock_out => clock_out
);

-- Clock process definitions
clk_process :process
begin
clk <= '0';
wait for clk_period/2;
clk <= '1';
wait for clk_period/2;
end process;

-- Stimulus process
stim_proc: process
begin
wait for 100 ns;
reset <= '1';
wait for 100 ns;
reset <= '0';
wait;
end process;

END;
```

Testbench Waveform for 1Khz Clock divider from 50MHz

clock input


Name
Value
clk
0
reset
0
clock_out
1
clk_period
20000 ps
500.200000 us
1,500.200000 us
0 us
500 us
1,000 us
1,500 us
2,000 us
2,500 us
3,000 us
20000 ps
1,000.000000 us
-500 us
0 us
500 us
1,000 us
1,500 us
2,000 us
2,500 us